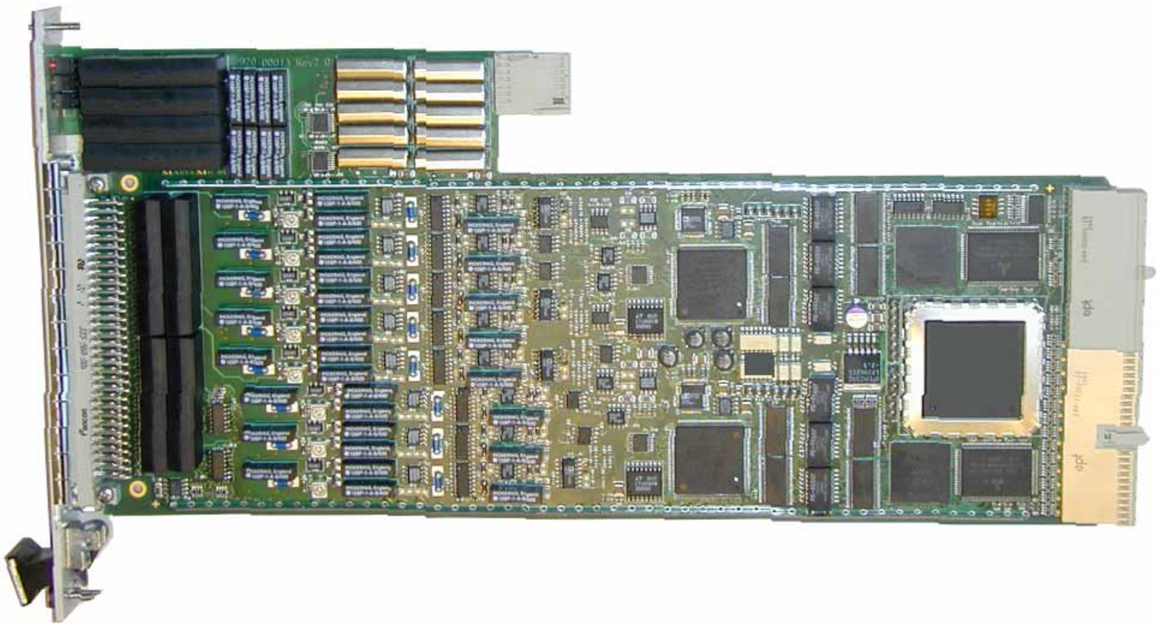
ROHDE & SCHWARZ

USER MANUAL



Analyzer Module

TS-PAM

User Manual

for ROHDE & SCHWARZ Analyzer Module TS-PAM

4th Issue / 11.05 / D 1152.3808.12

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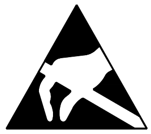

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Annex to Certificate Registration No.: 001954 QM ST

Rohde & Schwarz GmbH & Co. KG

Mühldorfstrasse 15
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Organizational unit/site	**Scope**
ROHDE & SCHWARZ GmbH & Co. KG Service Centre Cologne **ROHDE & SCHWARZ Systems GmbH** Graf-Zeppelin-Strasse 18 D-51147 Köln	Technical services in the field of measuring/communication techniques maintenance/repair calibration training technical documentation Development, production, systems
Rohde & Schwarz FTK GmbH Wendenschloßstrasse 168 D-12557 Berlin	Design and Development, Production and Sale of Communication Equipment, Installations and systems
Rohde & Schwarz GmbH & Co. KG Kaikenrieder Strasse 27 D-94244 Teisnach	Design and Development, Production, Sales, Services of Electronic-Measurement and Communication-Equipment and Systems
Rohde & Schwarz závod Vimperk s.r.o. Spidrova 49 CZE-38501 Vimperk Tschechische Republik	Design and Development, Production, Sales, Services of Electronic-Measurement and Communication-Equipment and Systems
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If you have any technical queries about this Rohde & Schwarz equipment, our Hotline at the Support Center of Rohde & Schwarz Sales-GmbH will be glad to help.

Our team will discuss your queries and look for solutions to your problems.

The Hotline is open Mondays to Fridays from 08.00 to 17.00 hrs.

For queries outside office hours, you can leave a message or send a note via fax or email. We will then get back to you as soon as possible.

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1 Applications

1.1 General

This manual describes the function and operation of the Analyzer Module TS-PAM (wave form analyzer) for use in the Test System Versatile Platform CompactTSVP. The hardware is designed as a CompactPCI module which occupies only one slot in the front side of the TSVP. The accompanying Rear I/O Module TS-PDC (DC/DC Transformer Module) is plugged into the same slot on the back side.

The following analyses are possible using the Analyzer Module TS-PAM and the Signal Analysis Library:

- Voltage and voltage changes with different qualifications
- Time measurements
- Events
- Wave-form comparison

The wave form analyzer is able to record electrical signals on two measuring paths (channels) at a high sampling rate of 20 MHz or on up to eight measuring paths (channels) in the „Scan“operation (quasi simultaneous) at a the low sampling rate of 5 MHz. The signals can be evaluated after acquisition with respect to parameters such as voltage, time, frequency, events. The measurement options can, in many cases, replace a digital voltmeter (DVM), a timer/counter or a digital oscilloscope. The Analyzer Module TS-PAM covers the application range above a fast sampling voltmeter (e.g. TS-PSAM or data acquisition module with scanner).

A wide range of trigger options for acquisition of the correct measuring interval and automatic analysis options in the actual production environment, where no optical evaluation of the signals can take place, ensure the reproducibility of the measurements.

The Test System Versatile Platform CompactTSVP TS-PCA3 allows you to plug in measuring and control modules according to industry standard CompactPCI or PXI. Apart from this, Rohde & Schwarz modules use an expanded printed circuit board format and have access to a special analog measurement bus.

1.2 Features of the TS-PAM

Features TS-PAM
Two fully independent, floating acquisition units with working voltage up to 125 VDC
Acquisition modes with up to 8 single-ended or 4 differential channels
High sampling rate 20 MSamples/s for two channels
Multi channel signal recording for up to 8 channels at 5 MSamples/s
Synchronous acquisition of 8 programable comparator signals and PXI-trigger additionally
Wide dynamic range with 14 bit resolution
Input ranges ±0.2 VDC up to ±100 VDC (125 V max.))
3:1 relay multiplexer per channel
2 x 1 MSamples memory depth
Analog and digital trigger signals
Analog measurement bus access to 8 bus lines
Selftest capabilities
Soft front panel support for direct operation
LabWindows/CVI driver support
GTSL test software library in DLL format

Table 1-1 Features TS-PAM

1.3 Features of the TS-PDC Module

The Rear I/O Module TS-PDC is used as a floating DC voltage source for the Analyzer Module TS-PAM . It contains two identical DC/DC converters. The following floating voltages are obtained from an input voltage of 5 VDC:

– +15 VDC ±5%, 0.5A (2x)
– -15 VDC ±5%, 0.5A (2x)
– +5 VDC ±5%, 0.5A (2x)
– +3.3 VDC ±5%, 0.25A (2x)

2 View

Figure 2-1 shows the Analyzer Module TS-PAM without the accompanying Rear I/O Module TS-PDC.

The Rear I/O Module TS-PDC is shown in Figure 2-2 .

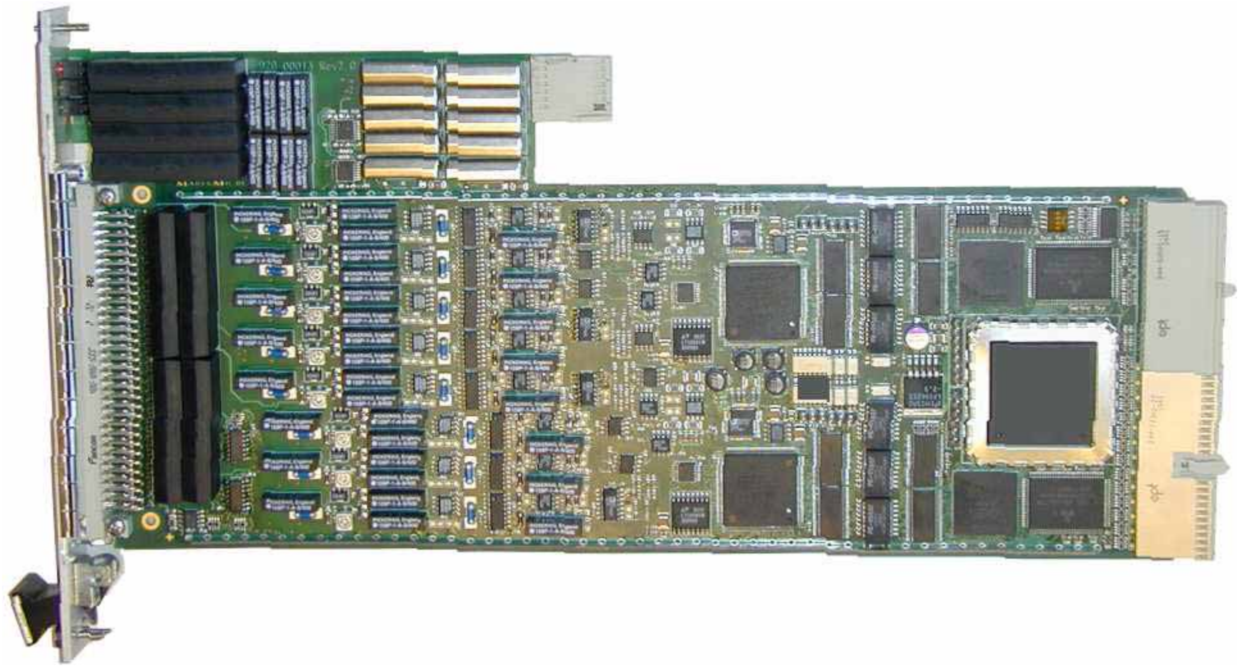

Figure 2-1 View of the TS-PAM

Figure 2-2 View of the Rear I/O Module TS-PDC

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3 Block Diagram

Figure 3-1 shows the simplified functional block diagram of the Analyzer Module TS-PAM and the Rear I/O Module TS-PDC in the CompactTSVP .

Figure 3-2 shows the block diagram of the Analyzer Modules TS-PAM .

Figure 3-3 shows the block diagram of the Rear I/O Module TS-PDC.

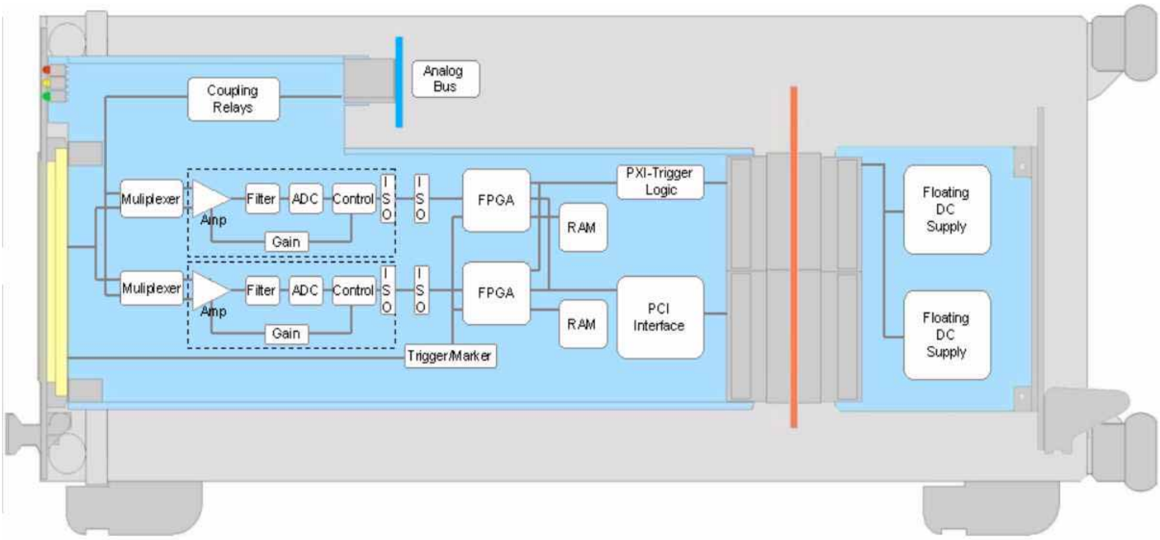

Figure 3-1 Block diagram of TS-PAM with TS-PDC in the CompactTSVP

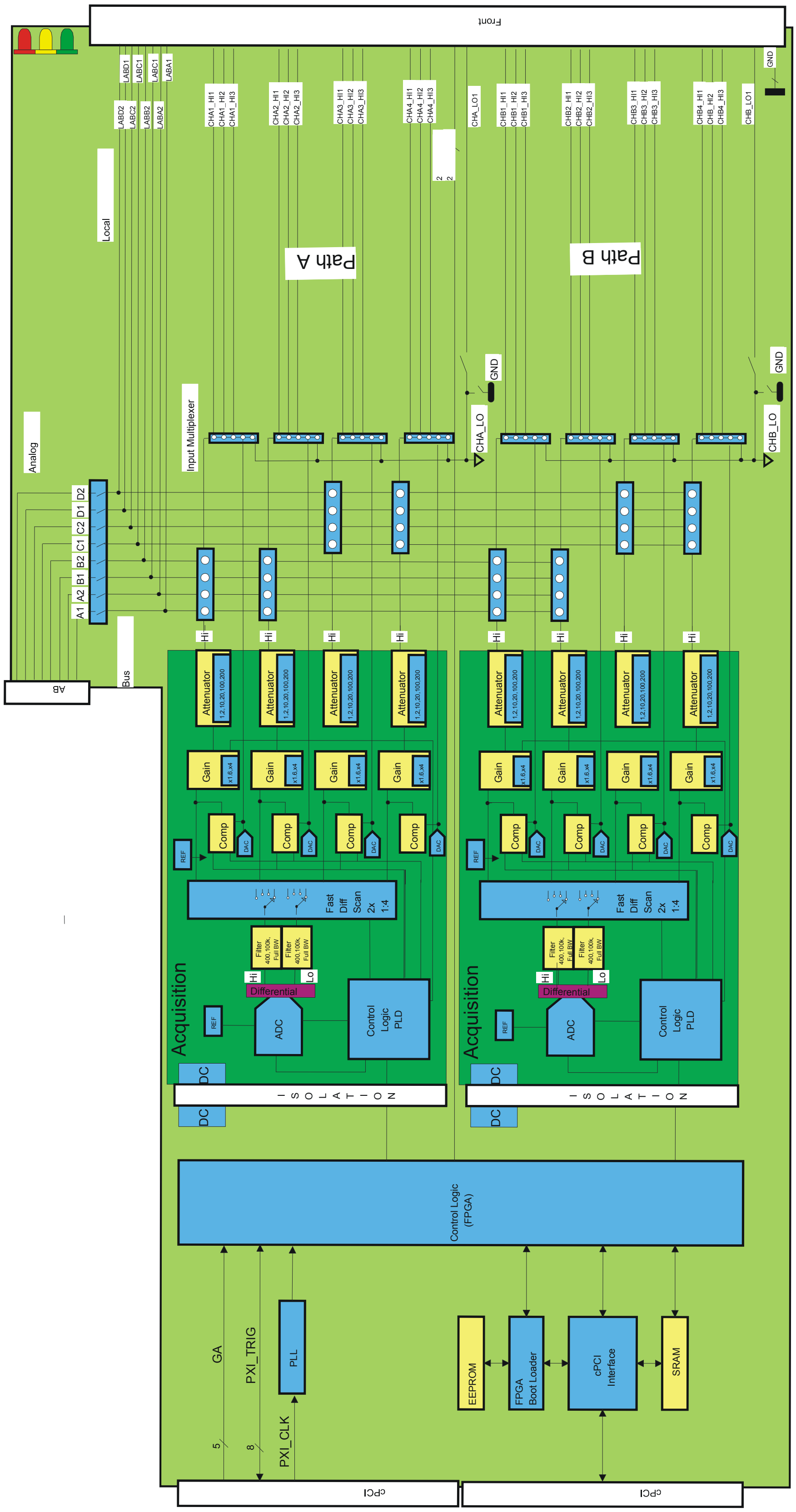

Figure 3-2 Block diagram of Analyzer Module TS-PAM

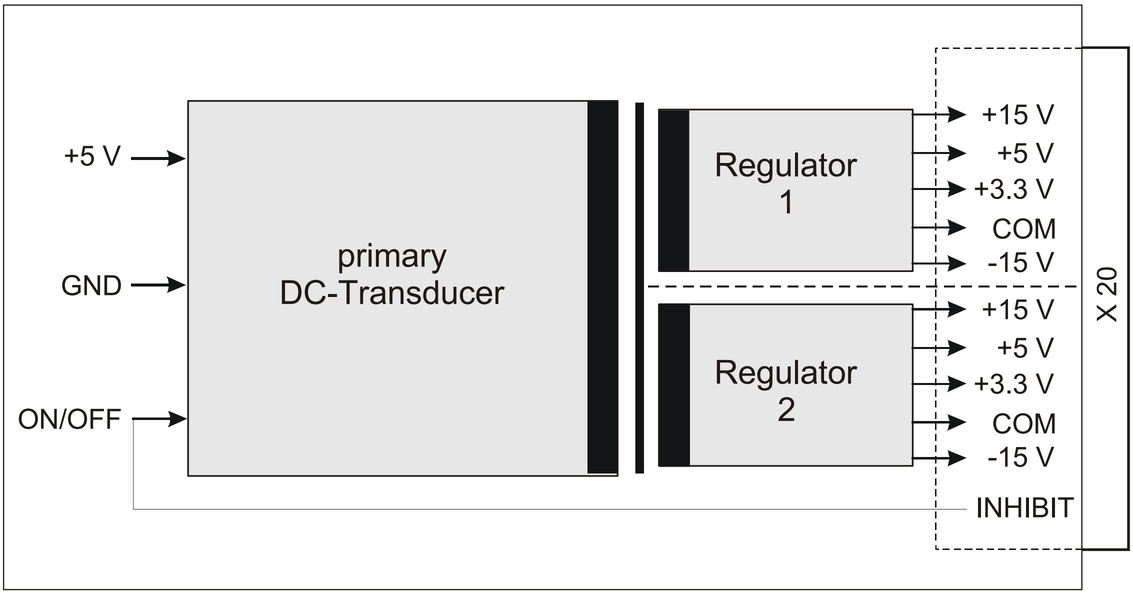

Figure 3-3 Block diagram of Rear I/O Module TS-PDC

4 Design

4.1 Mechanical Design of the Module TS-PAM

The Analyzer Module TS-PAM is designed as a **long cPCI plug-in module** for mounting in the front of the CompactTSVP. The insertion depth is 300 mm. The board height of the module is 4 HU.

In order to ensure that it is inserted correctly into the CompactTSVP, the front panel is furnished with a locating pin. The module is secured in place with the two retaining screws on the front panel. Front connector X10 is used for connecting the UUTs. Connector X30 connects the TS-PAM module to the analog bus backplane in the CompactTSVP. The Connectors X20/X1 connect the TS-PAM module to the cPCI backplane/PXI control backplane.

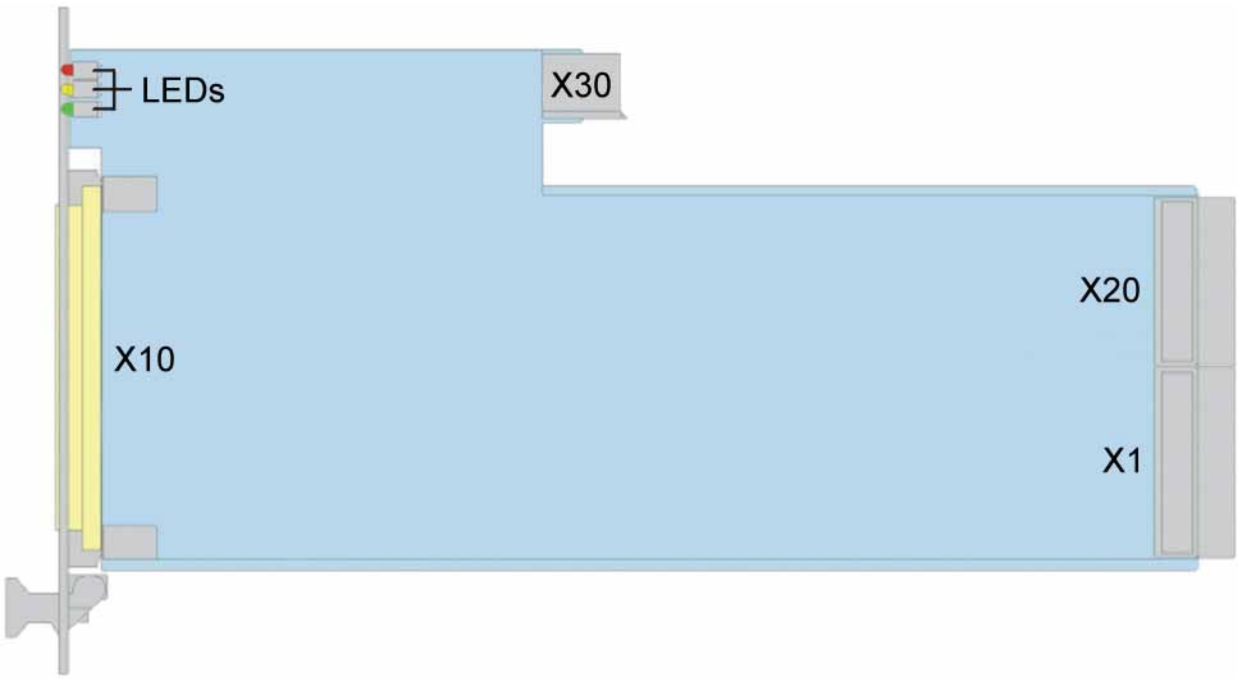

Figure 4-1 Arrangement of the connectors and LEDs on the module TS-PAM

Name	Use
X1	cPCI connector
X10	Front connector
X20	cPCI connector
X30	Analog bus connector

Table 4-1 Connectors on the TS-PAM

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4.2 Display elements of the module TS-PAM

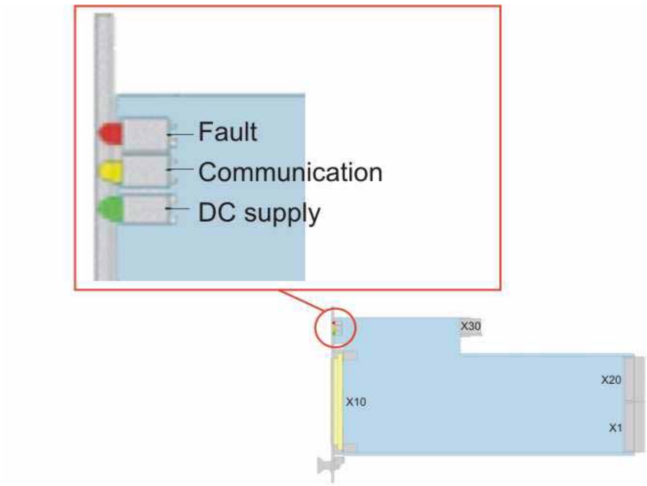

Figure 4-2 Arrangement of the LEDs on the module TS-PAM

On the front side of the module TS-PAM there are three LEDs which show the current status of the module. The LEDs have the following meaning:

LED	Description
red	Fault condition: Lights up when a fault is detected on the TS-PAM module during the power-on test after the supply voltage is switched on. This means that there is a hardware problem on the module. (also see section 8: Self-test)
yellow	Communication: Lights up when data is exchanged across the inter-face.
green	Supply voltage OK: Lights up when all necessary supply voltages are present (incl. the TS-PDC voltages).

Table 4-2 Display elements on the module TS-PAM

4.3 Mechanical Design of TS-PDC

The module TS-PDC is a **Rear I/O Module** for insertion in the back side of the CompactTSVP. The printed circuit board height of the module is 3 HU (134 mm). The module is attached with both fastening screws of the front panel. The connector X20 connects the module TS-PDC with the extension back panel in the CompactTSVP. The module TS-PDC must always use the corresponding rear I/O slot for the main module (e.g. module TS-PAM).

WARNING!

The module TS-PDC must always be plugged into the corresponding rear I/O slot (same slot code) of the module TS-PAM . If it is not correctly plugged in (e.g. cPCI/PXI standard modules in the front area) both modules may be destroyed.

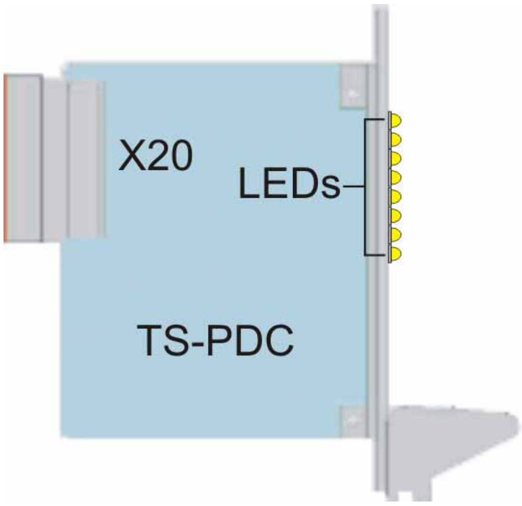

Figure 4-3 Arrangement of the connector and LEDs on the module TS-PDC

Name	Use
X20	Extension (Rear I/O)

Table 4-3 Connector of the module TS-PDC

4.4 Display Elements of the Module TS-PDC

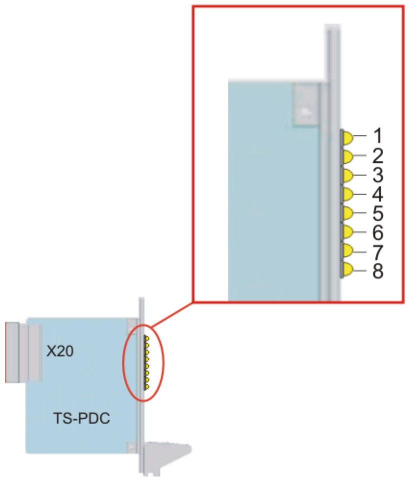

Figure 4-4 Arrangement of the LEDs on the module TS-PDC

Eight light-emitting diodes (LEDs) are located on the front of the TS-PDC module to show the current status of the generated supply voltages. The individual LEDs have the following meanings:

LED	Description
1, lights up	+15 VDC (CHA), present
2, lights up	+5 VDC (CHA), present
3, lights up	+3.3 VDC (CHA), present
4, lights up	-15 VDC (CHA), present
5, lights up	+15 VDC (CHB), present
6, lights up	+5 VDC (CHB), present
7, lights up	+3.3 VDC (CHB), present
8, lights up	-15 VDC (CHB), present

Table 4-4 Display elements on the module TS-PDC

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5 Description of Functions

5.1 Description of Functions of the Module TS-PAM

The Analyzer Module TS-PAM is a signal analyzer similar to a multi-channel digital storage oscilloscope (DSO). It has two acquisition units, which can be operated separately or synchronized. Thus, the TS-PAM functions as two separate digital oscilloscopes or as a digital oscilloscope with twice the number of channels. The two acquisition units are separated according to control/software as well as potential. Because each path is floating, each path can be connected to a different potential and measured there with high accuracy of measurement. Naturally the paths can also be grounded, as with digital oscilloscopes.

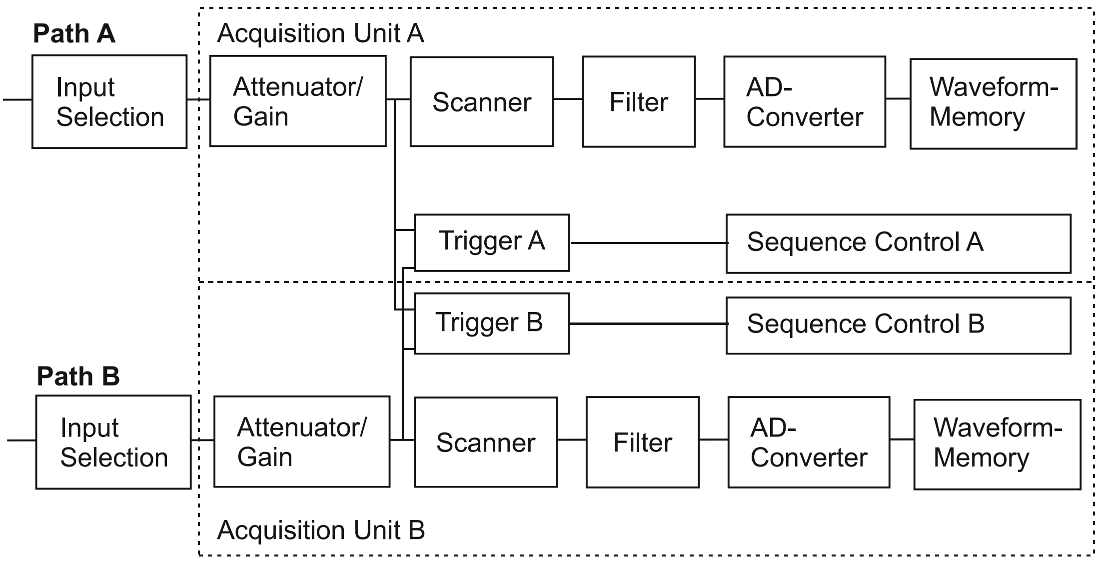

Figure 5-1 Functional blocks of TS-PAM

5.1.1 Acquisition Unit

Each acquisition unit has four channels with individually adjustable gain.

In single-channel mode, two channels or one channel and the floating reference potential can be statically selected. The A/D converter measures the difference signal with maximum sample rate. With two acquisition units, two signals with conversion rates up to 20 MHz can be recorded, which corresponds to a sampling period of 50 ns.

In multi-channel mode, two to four signals of a path can be quasi-simultaneously acquired. The channels are scanned and recorded with time offset. At the maximum sampling frequency of 20 MHz, the effective sampling frequency for four aquisition channels is 5 MHz, the interval delta time (offset) is 50 ns. You can select whether the difference between individual channels or the difference of the channels against the floating reference potential is to be measured. With two acquisition units, a total of eight channels can be simultaneously recorded.

Because in most cases, the floating potentials can serve as a reference or even be measured single-ended against GND, all eight channels can be used and there is seldom need to take the difference between two channels. The reference potential of a path is connected to GND or different reference potential of the unit under test. With particularly sensitive units under test, it is possible that the test signal may be distorted if the reference potential of a path is connected directly to the unit under test (cause: The reference potential has a higher capacitance and higher leakage current to GND compared to an input). This can be avoided by using two channels of a unit and measuring fully differential with two high-impedance inputs.

In the standby state after software initialization, each acquisition unit is connected to GND through a relay and a resistor, for reasons of signal technology. During floating operation, this relay is automatically opened when a connection is made to a front connector pin or to the analog bus. During grounded operation, when the GND relay remains closed, care must be taken that the relay and resistor are not overloaded.

5.1.2 Inputs and Measurement Ranges

Each measuring channel can be switched with relays to three input channels, to four lines of the local analog bus LABxy, to the reference potential CHA_LO or CHB_LO or to the analog output for the trigger threshold of the comparator. If the local analog bus line is used as an additional input, 4 x 8 = 32 pins on the connector X10 can be measured without having to use a relay in the adapter or an additional plug-in card.

If the local analog bus LAB is connected with the global analog bus AB, up to eight channels can be simultaneously measured and there is access to an almost unlimited number of measuring points (90 channels per plug-in module TS-PMB). Here too, single-ended and differential measurements are possible.

Each measuring channel has a programmable input divider and measurement amplifier. With nine measurement ranges from 0.2 V to 100 V, small to high voltages can be optimally acquired with 14 bit resolution. In the small measurement ranges, instead of the normal input impedance of 1 MΩ, higher impedances can be measured. Because the floating measuring technique is used, the measuring accuracy of the small ranges is also possible for small signals on high potential.

The maximum permitted rated voltage between arbitrary pins is 125 V.

Measurement range	Resolution	Input impedance
± 100 V	15 mV	1 MΩ
± 50 V	7.5 mV	1 MΩ
± 20 V	3 mV	1 MΩ
± 10 V	1.5 mV	1 MΩ
± 5 V	0.75 mV	1 MΩ or >10 MΩ selectable
± 2 V	0.3 mV	1 MΩ or >10 MΩ selectable
± 1 V	0.15 mV	1 MΩ or >10 MΩ selectable
± 0.5 V	75 µV	1 MΩ or >10 MΩ selectable
± 0.2 V	30 µV	1 MΩ or >10 MΩ selectable

Table 5-1 Measurement ranges

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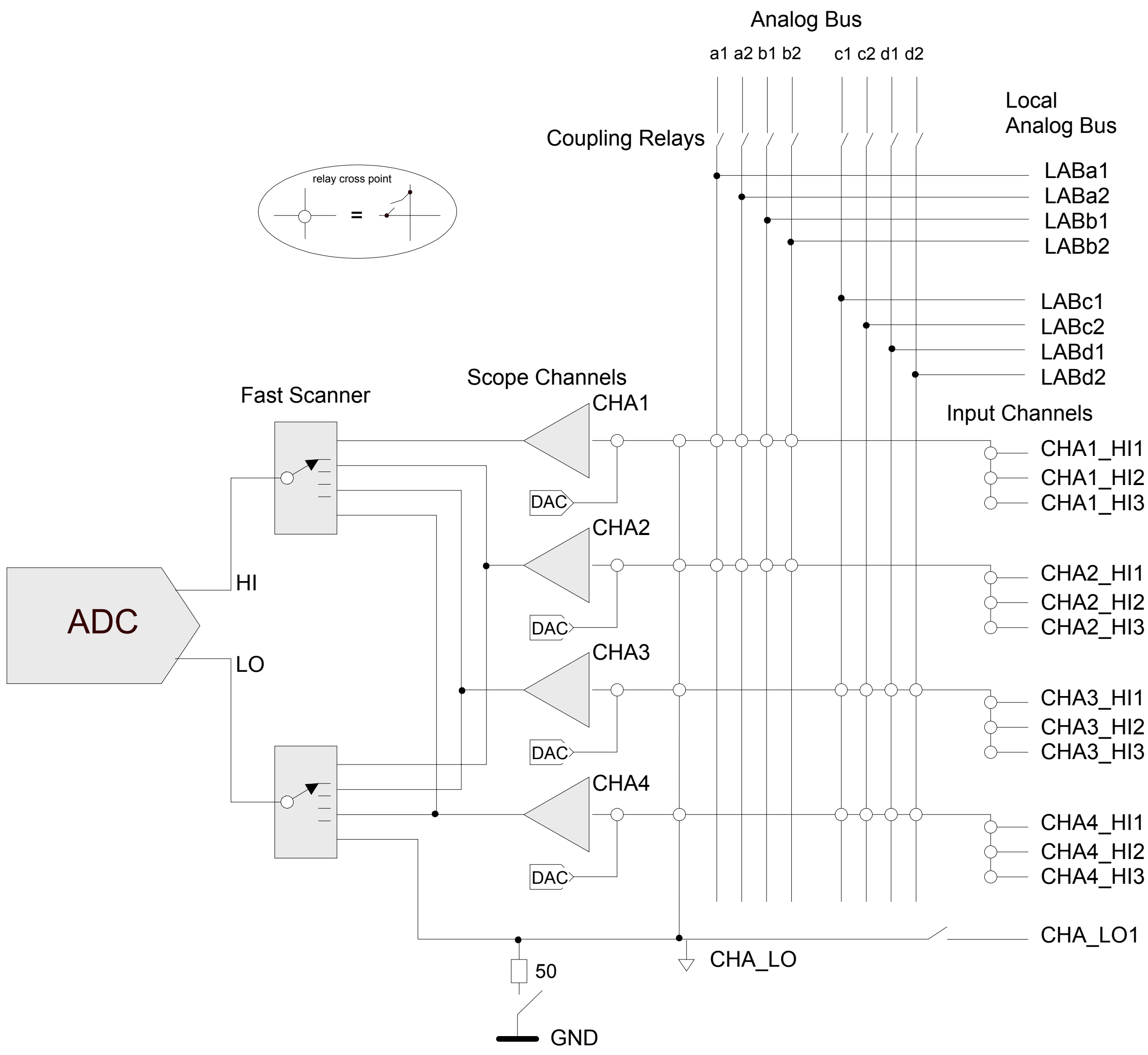

Figure 5-2 Signal inputs and scanner of an acquisition unit (path A)

Signals can be recorded within the input bandwidth. Similarly to digital oscilloscopes, no anti-aliasing filter is provided. For signal conditioning, hardware low pass filters can be connected in series.

The inputs are DC coupled. An AC coupling can be done by connecting an external capacitor in series. The time constant is optimized by the appropriate selection of R and C on the measuring frequency and the desired transient time.

Four programmable analog sources (DAC) per acquisition unit set the trigger threshold of the comparators of each channel and can be connected as a control voltage source for the self-test to the analog bus. The programming is according to the value of the trigger threshold and the set measurement range.

5.1.3 Timing Control, Scanner

The sampling rate can be varied so that slow or fast signals are optimally acquired and stored in the wave form memory. Because the timing of each acquisition unit can be independently set, slow and fast signals can be simultaneously optimally acquired, which results in a considerably better use of the wave form memory and effectively increases its depth.

Depending on whether the single-channel or multi-channel operating mode is used, the sampling rate can be max. 20 MHz or 5 MHz.

The precise time reference is derived from the 10 MHz PXI clock of the Test System Versatile Platform CompactTSVP.

5.1.4 Synchronization, Trigger

Each acquisition unit can be started through the software, through the test signals, external trigger inputs or PXI trigger inputs (from other modules). For triggering through the test signals, analog comparators with programmable threshold and selectable flanks are used.

Trigger output signals can trigger other modules on the front connector X10 or on the PXI trigger bus. Through the pins XTO1 and XTO2, the trigger time points of both acquisition units or the eight analog trigger signals can be fed out. These signals can also be fed to the eight PXI trigger lines.

The acquisition units can begin the recording synchronously, independently or initiated by the other acquisition unit. The storage in the wave form memory can be done pre- or post-trigger.

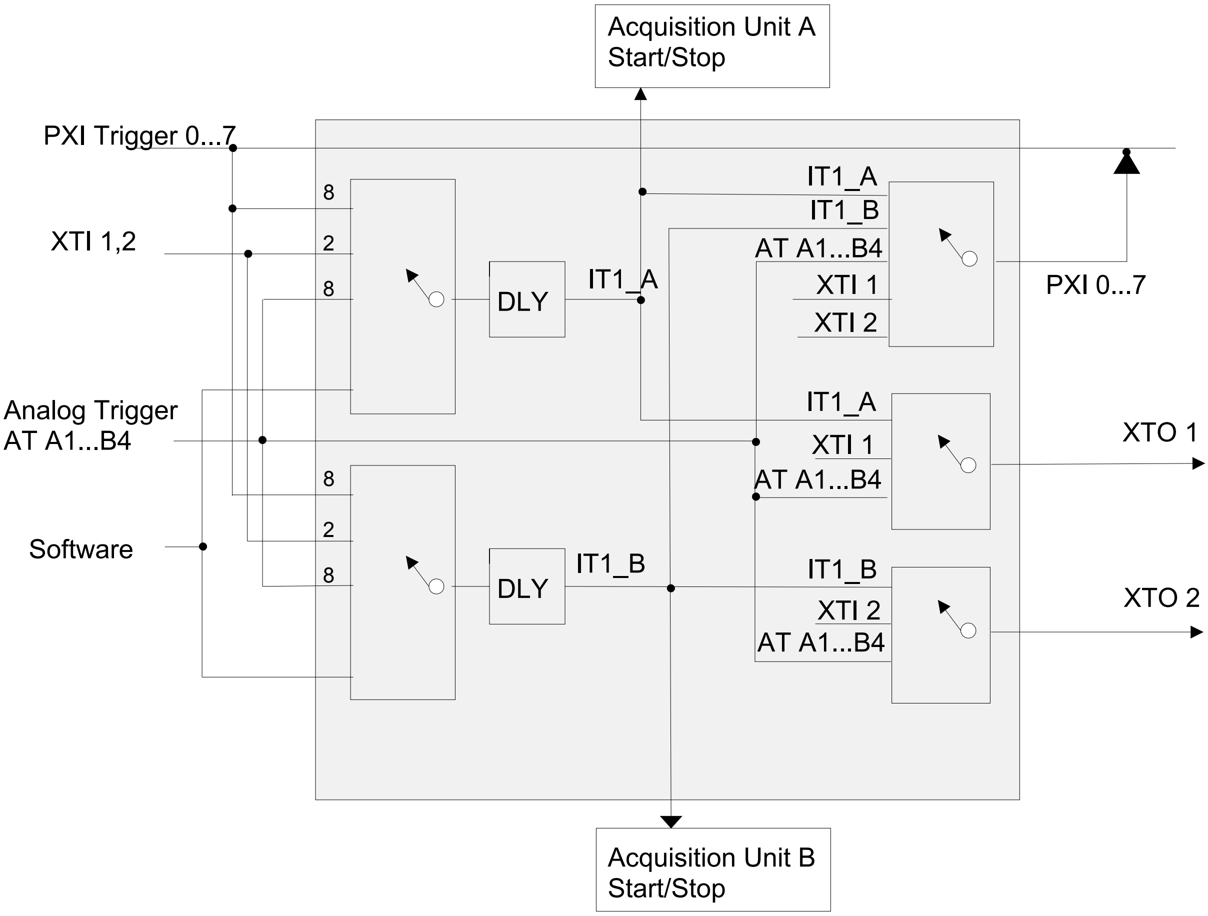

Figure 5-3 Trigger unit

5.1.5 Memory

The wave form memory contains 1 MSamples (of 32 Bit width) per acquisition unit. This means that in the single-channel mode, two channels (each acquisition unit) can record a maximum of 1 MSamples each. In the multi-channel mode, eight channels up to a depth of 256 ksamples each can be measured. In addition to the analog values, the trigger information from the PXI-Bus and the analog comparators is also recorded.

5.1.6 Signal processing, Filter

The measuring channels are broadband and have, like digital oscilloscopes, no specific anti-aliasing filters. For noise suppression, a 100 kHz or 400 Hz filter can be connected in the path. It has to be observed that the filters are arranged behind the measuring scanner. The filters only function correctly if the filter cut-off frequency is distinctly higher than the scan frequency. Otherwise, a distortion of the measurement value can occur up to an identical test signal of all channels.

An additional filtering can be obtained with the digital filter (low pass filter with cut-off frequency 0.2 x sampling frequency).

Additional special filter features can be implemented with software by processing of the waveform arrays with commercially available programs.

5.1.7 Analog Bus Access

Each input channel has direct access to four local analog bus lines and through coupling relays to the global analog bus. Thus, a total of eight channels can be simultaneously connected to the analog bus. Instead of an input channel, the floating reference potential CHA_LO or CHB_LO can be switched to the analog bus. In this way, the measuring channels can measure signals from other switch modules, and signals to the connector X10 can also be connected to other measuring modules.

When there is signal feed through the analog bus and other cards, it must be noted that the best signal quality is obtained only for short signal paths. Signals to the connector X10 can therefore be best measured.

5.1.8 Measuring Functions

The acquisition units can record analog signals and at the same time digital trigger signals within a given time. An analysis of the wave forms can be done with the Signal Analysis Library (see Software Analysis Library in Section 7.3).

5.1.9 Particulars of Floating Measurements

To make optimum use of the possibilities of floating measurement of TS-PAM, it is important to look at the grounding. The unit under test **or** the measuring instrument must be grounded in order to obtain reproducible, stable measuring results. Only with very slow measuring techniques (battery operated hand multimeters) the hum can be equalized by decelerating averaging. For fast and accurate measurements, one must give some thought to the grounding. It is important here to only provide a single grounding point. See examples Figure 5-4 to Figure 5-8 .

a) **Simple Single-ended Grounding**

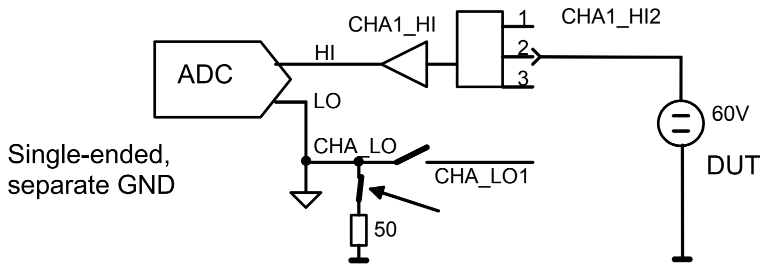

Figure 5-4 Grounding procedure “Simple Single-ended Grounding”

In the simplest case (Figure 5-4) with low accuracy requirements, grounding is done “somewhere”, i.e. the unit under test is grounded in the fixture, the measuring unit is internally connected to GND.

Advantage: Only the test signals are considered; the grounding is connected in some way. The connection becomes very simple. If the signals are fed through the analog bus, you save one bus line for the GND.

Disadvantage: Low accuracy, particularly for signals in the magnitude of 100 mV and lower.

When there is a small difference in the grounding potentials, transient currents flow which distort the measurement. The LO input of the measuring unit is not arbitrarily low resistant but connected to ground through approx. 50 Ω; faults up to 50 mV can be caused by derivative currents. This type of connection has the hidden danger that one may inadvertently place a grounded voltage on CHA_LO. Thus, there may be a higher current which destroys the relay contacts. Therefore, there is here a PTC resistor with a approx. 50 Ω resistance built in, which limits this current. However, it must be ensured that neither the max. current of the GND relay (500 mA) nor the switching power of 15 W are exceeded.

Measurement a) is used for digital oscilloscopes and non-differential A/D converter cards. There is no option to separate the acquisition unit from GND for these devices.

b) **Single-ended, Grounding on the Unit under Test**

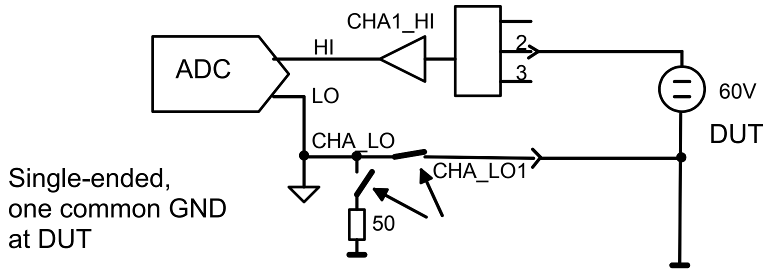

Figure 5-5 Grounding procedure “Single-ended, Grounding on Unit under Test”

With this wiring (Figure 5-5), the floating character of the acquisition unit of TS-PAM is used to ground only on the low-resistance ground point of the unit under test (grounding only on one point).

Advantage: Accurate measurements even at low voltages, no ground loops or potential differences, because there is only a single ground point.

Disadvantage: The CHA_LO must be specifically connected with relays and wired in the fixture. When there is signal feed through the analog bus, an additional bus line is necessary.

c) **Floating with Potential as Reference**

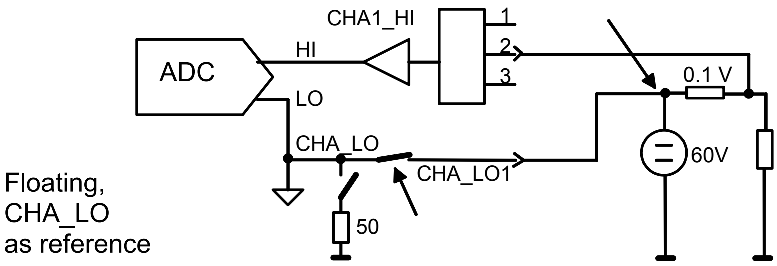

Figure 5-6 Grounding procedure "Floating with Potential as Reference"

With this wiring, (Figure 5-6) the measuring unit can be operated on a deviating, higher potential (instead of being grounded).

Advantage: Despite a voltage of 60 V e.g. , the smallest ranges and not the 100-V range can be used to measure the current. The common mode suppression is nearly ideal using the floating measuring technique.

Disadvantage: The „cold" connection CHA_LO is not exactly equal to the „hot" signal connection (CHA1_HI2). The LO connection has a greater capacity (to the order of 1 nF) to ground and exhibits greater leak currents between LO and GND. In most cases this capacity can change the signal on the unit under test. Therefore LO must be applied to a low resistant point of the unit under test. In the example of the current measurement by the voltage drop at a resistor, this is the side facing the source.

Digital oscilloscopes and non-differential A/D converter cards must use two channels for this. Otherwise, they can only measure in the inaccurate large measurement ranges (60 V). Even differential A/D converter cards must use the large measurement ranges and lose accuracy.

d) **Differential measurement with two Channels**

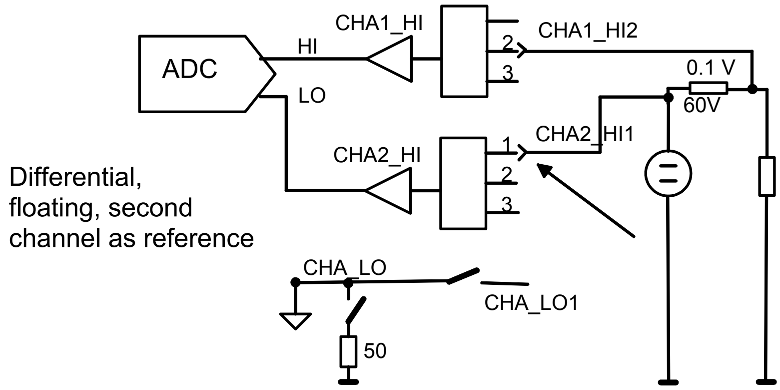

Figure 5-7 Grounding procedure “Differential Measurement with two Channels”

Similarly to c), with this wiring (Figure 5-7), measurement can be done on a different potential. However, a high-resistance separate channel with low capacitance is used as reference.

For reproducible measurements the input ranges with 1 MΩ input resistance must be used. This reistance must be selected specifically in the small measuring ranges.

Reason: Since the acquisition unit is operated here without direct reference potential, leak currents of the operational amplifier cannot otherwise flow to the reference potential CHA_LO.

Advantage: The high-resistance input from CHA2_HI1 distorts the signal on the unit under test very little. Measurement can be done in the more accurate small measurement ranges.

Disadvantage: An additional channel is necessary.

e) **Differential Measurement at High Reference Potential**

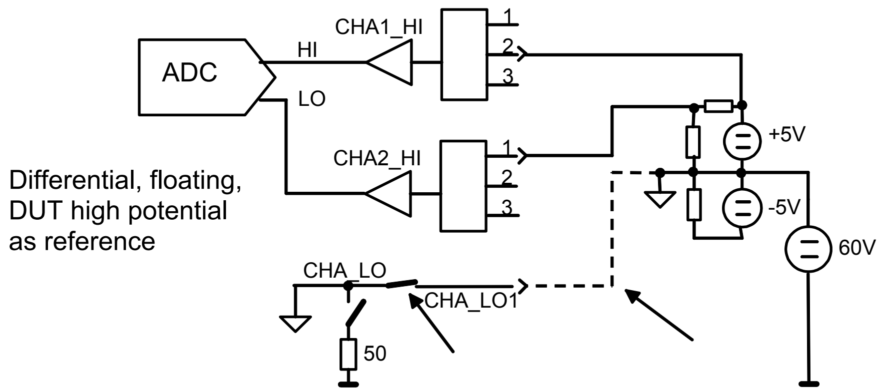

Figure 5-8 Grounding procedure “Differential Measurement at High Reference Potential”

The wiring as in Figure 5-8 is optimally suited when a unit under test has a larger portion of the circuit at a higher reference potential than the other grounded circuit. The reference potential of the acquisition unit is connected to the reference potential of unit under test (60 V in the example, broken line).

Advantage: All measurements can be carried out in the small, more accurate measurement ranges. Single-ended measurements against the reference potential or differential measurements between various signals of the high potential can be carried out. Fewer analog bus lines are necessary.

Disadvantage: It must be noted which signals belong to the high reference potential and a line for this provided. There is danger of a short circuit between GND and high reference potential.

It must be ensured that one does not inadvertantly close the GND relay and thus cause a short circuit.

5.1.10 Information for Operation with Dangerous Voltages

The following voltages are considered “dangerous live” under EN 61010-1.

- 70 V DC
- 33 V AC eff
- 46.7 V AC peak

CAUTION!

When operating the Analyzer Module TS-PAM above these voltage limits, the instructions under EN 61010-1 must be followed.

The Analyzer Module TS-PAM and the Test System Versatile Platform CompactTSVP are designed for a maximum voltage of 125 V between floating measuring components, analog buses and GND. It must be ensured that this limit is not exceeded at any time, even at summation of the voltages, even through alternating signals.

Figure 5-9 shows some typical permissible voltage configurations between analog buses and ground.

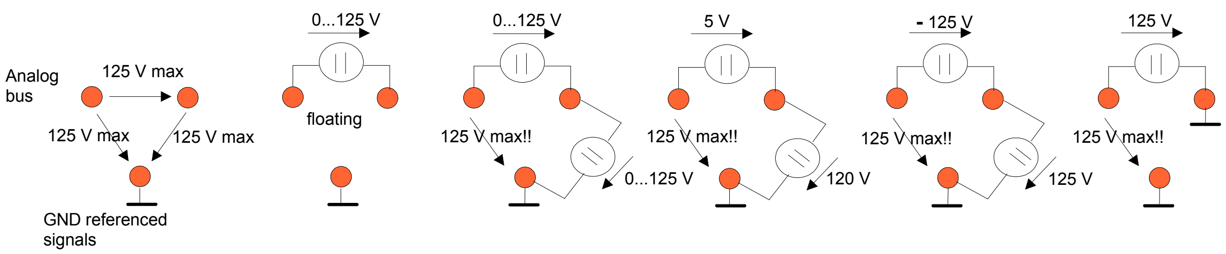

Figure 5-9 Permitted voltages on analog bus lines

For reasons of fire safety, it is recommended in EN 61010-1 that for DC-sources, the current or the rating be limited to 150 VA.

5.1.11 Power Supply

The digital portion of the Analyzer Module TS-PAM is supplied with power of +5 V and +3.3 V of the CompactPCI Bus. The two floating measuring portions are each supplied with a set of floating voltages, +5 V, +3.3 V, +15 V, -15 V from the rear I/O module TS-PDC (DC/DC converter). The associated capacity is taken from the 5-V-CompactPCI supply.

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5.2 Description of Functions of the Module TS-PDC

The Rear I/O Module TS-PDC is configured as a primary reference DC/DC converter. The input voltage (5 VDC) is transfered to two secondary potentials and rectified to the nominal voltage by line controllers. The status of the output voltage is displayed in each case by an LED.

The following DC voltages are generated:

- +15 VDC, 0.5A (2x)
- -15 VDC, 0.5A (2x)
- +5 VDC, 0.5A (2x)
- +3.3 VDC, 0.25A (2x)

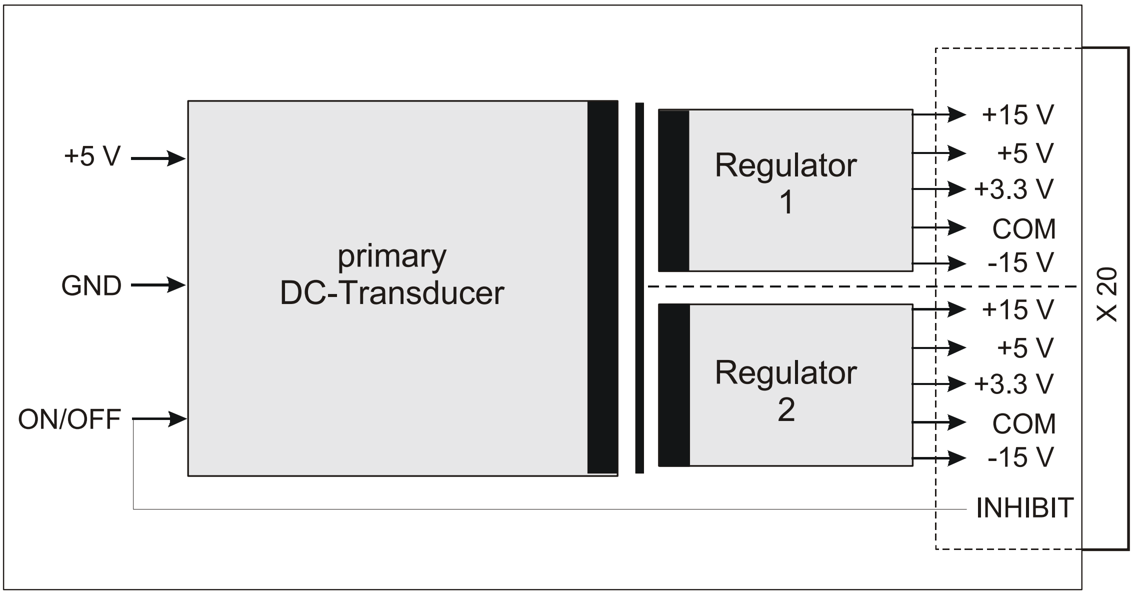

Figure 5-10 Block schematic diagram of Rear I/O Module TS-PDC

6 Commissioning

6.1 Installation of the Plug-in Module

- Power down and switch off the CompactTSVP.
- Select a suitable front slot (slots 5-15 possible).
- Remove the corresponding front panel portion from the TSVP chassis by loosening the two screws.

WARNING!

Check the backplane connectors for bent pins! Any bent pins must be straightened!
Failure to do this may permanently damage the backplane!

- Apply moderate pressure to insert the plug-in module (use locating pin to attach).

WARNING!

To insert the plug-in module, use both hands to guide carefully into the backplane connectors.

- The module is correctly located when a distinct “stop” can be felt.
- Tighten the two retaining screws on the front panel of the module.

WARNING!

Install the associated TS-PDC rear I/O module as described in Section 6.2 .

6.2 Installation of the Module TS-PDC

To install the plug-in module, proceed as follows:

- The TS-PAM module must have been installed beforehand.
- Select the corresponding rear I/O slot for the TS-PAM module.
- Remove the corresponding rear panel portion from the CompactTSVP chassis by loosening the two screws.

WARNING!

Check the backplane connectors for bent pins! Any bent pins must be straightened!
Failure to do this may permanently damage the backplane!

- Push in the plug-in module using moderate pressure.

WARNING!

To insert the plug-in module, use both hands to guide carefully into the backplane connectors.

- The module is correctly located when a distinct “stop” can be felt.
- Tighten the two retaining screws on the front panel of the module.

7 Software

7.1 Driver Software

For the functions of the signal recording of the Analyzer Module TS-PAM , a LabWindows IVI SCOPE driver is available. All other functions of the hardware are served by specific extensions of the driver. The driver is a component of the ROHDE & SCHWARZ GTSL software. All functions of the driver are fully documented in the online help and in the LabWindows/CVI Function Panels.

During driver installation, the following software modules are installed:

Module	Path	Comment
rspam.dll	<GTSL directory>\Bin	Driver
rspam.hlp	<GTSL directory>\Bin	Help file
rspam.fp	<GTSL directory>\Bin	LabWindows CVI Function Panel file, function panels for CVI development interface
rspam.sub	<GTSL directory>\Bin	LabWindows CVI attribute file. This file is required by some „function panels“.
rspam.lib	<GTSL directory>\Bin	Import Library
rspam.h	<GTSL directory>\Include	Header file for the driver

Table 7-1 Driver installation TS-PAM

NOTE:

To use the driver, the IVI and VISA libraries from National Instruments are necessary.

7.2 Soft Panel

For the Analyzer Module TS-PAM, there is a Soft Panel available (Figure 7-1). The Soft Panel is based on the LabWindows CVI driver. The Software Panel enables interactive operation of the module. The measured values are displayed graphically.

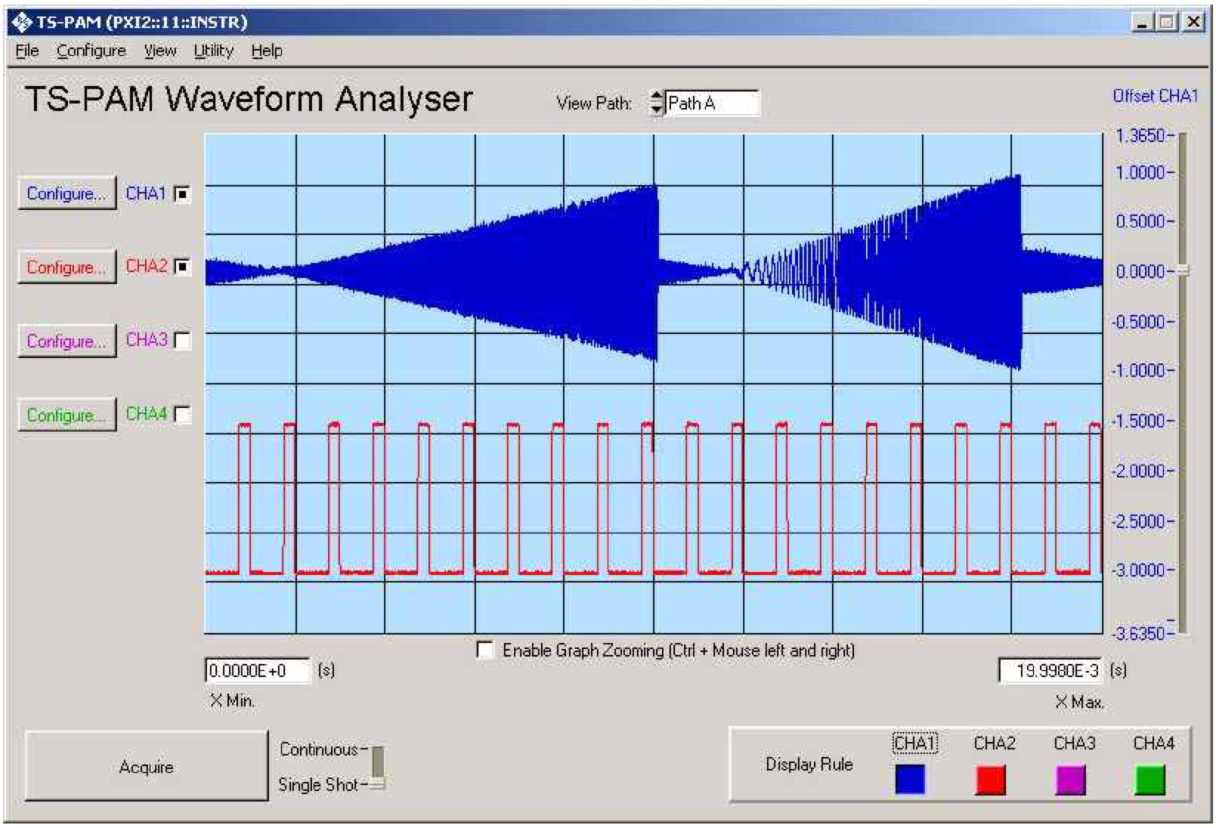

Figure 7-1 Soft Panel TS-PAM

The switching of the signal path of TS-PAM can be done through the Soft Panel (Figure 7-2).

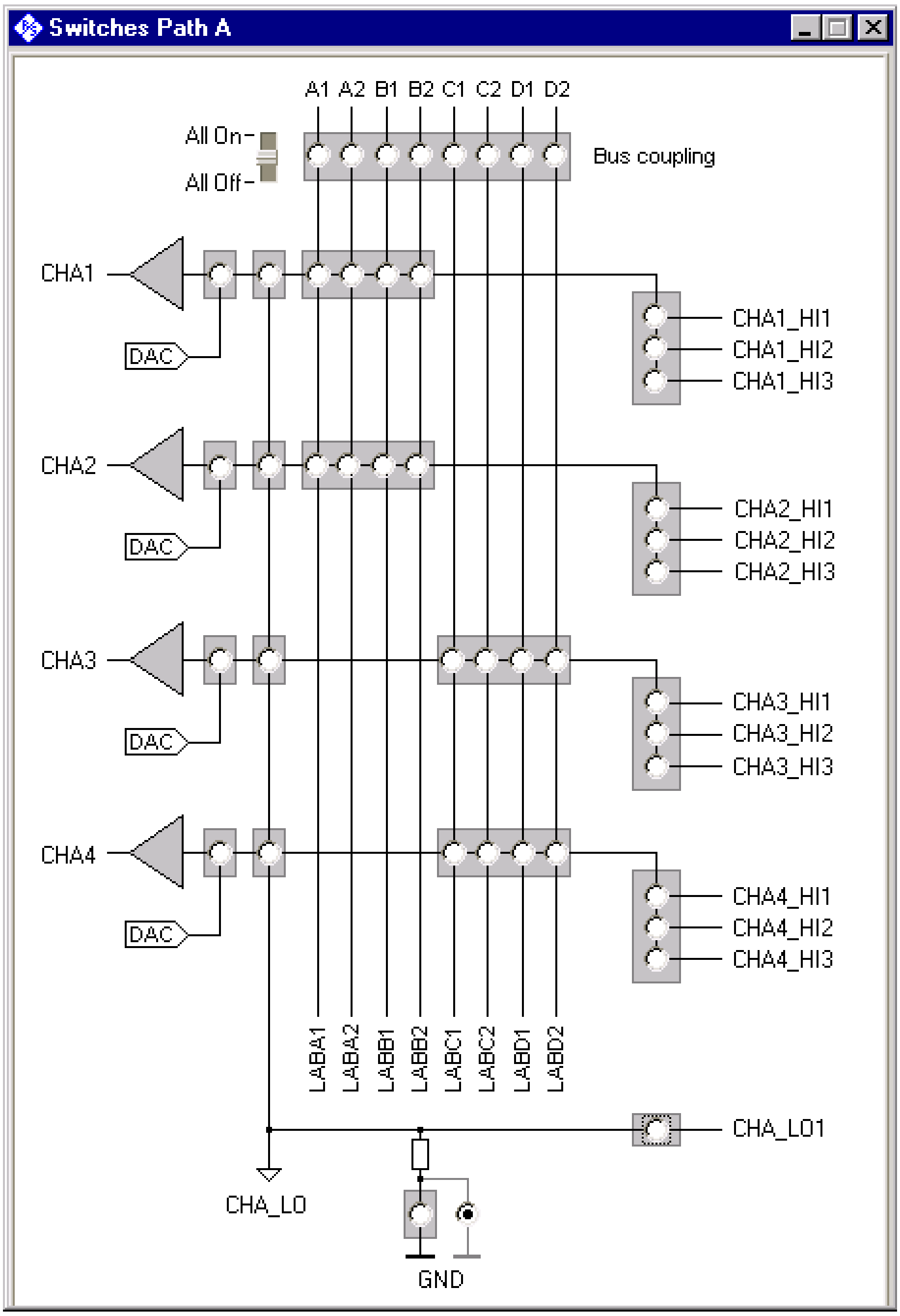

Figure 7-2 Soft Panel TS-PAM switching

7.3 Signal Analysis Library

The Signal Analysis Library offers functions for the analysis of the signals recorded by the Analyzer Module TS-PAM . The following signal parameters can be determined:

- Frequency, period
- Average value, RMS
- Rise and fall times
- Pulse width
- Maximum and minimum values (absolute and relative maxima/minima)
- Event counting (slopes, minima, maxima)
- Time measurement between two events

In addition, the Signal Analysis Library offers the following functions:

- Wave form comparison
- Calculation of reference wave forms
- Loading and saving of the wave forms as files
- Display of signal waves with reference curves and markers

Module	Path	Comment
siganl.dll	<GTSL directory>\Bin	Driver
siganl.hlp	<GTSL directory>\Bin	Help file
siganl.fp	<GTSL directory>\Bin	LabWindows CVI Function Panel file, function panels for CVI development interface
siganl.lib	<GTSL directory>\Bin	Import Library
siganl.h	<GTSL directory>\Include	Header file for the driver

Table 7-2 Installation of the signal analysis library

The analysis of audio signals is possible with the Audio Analysis Library TS-LAA. This library offers the following functions:

- RMS calculation
- Single/Multitone frequency response
- Distortion factor
- Filter (low-pass, high-pass, band-pass, band-stop, CCIR weighted/unweighted)

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- Windowing of the signal

7.4 Programming example TS-PAM

The following sample program shows the recording of a signal which contacts the connections CHA1_HI1 and CHA_LO1 on the front side connector.

```
/*

  This sample shows the acquisition of analog wave forms
  using the TS-PAM module.

  Error handling is not considered in this sample in order to
  keep it easy to read. The return status should be checked for
  VI_SUCCESS after each driver call.

*/

#include <ansi_c.h>
#include <userint.h>

#include "rspam.h"

int main (int argc, char *argv[])
{

  ViSession vi;
  ViStatus  status;

  ViReal64  * pWaveform = VI_NULL; /* pointer to wave form array */
  ViInt32   actualPoints;          /* number of samples returned from */
  ViReal64  initialX;              /* time of the first sample, relative
                                      to the trigger event */
  ViReal64  xIncrement;            /* time between two samples */

  /*
    Open a session to the device driver. The resource descriptor
    depends on the slot number of the TS-PAM module and must be
    adapted to the target system.
  */
  status = rspam_InitWithOptions ( "PXI1::13::0::INSTR",
                                   VI_TRUE,
                                   VI_TRUE,
                                   "Simulate=0,RangeCheck=1",
                                   &vi);

  /*
    Configure the acquisition time base for path A:
    Take a minimum of 20000 samples in 1 ms
    - Sample frequency is 20 MHz
    - Trigger delay = 0, i.e. no pre- or post-triggering
  */
  status = rspam_ConfigureAcquisitionRecordPath (vi, RSPAM_VAL_PATH_A,
                                                 1.0e-3, 20000, 0.0);

  /*
    Configure channel CHA1 for a signal between -5 V and + 5 V.
    The vertical range is 10 V (peak-to-peak), the offset is 0 V.
  */
  status = rspam_ConfigureChannel (vi, "CHA1", 10.0, 0.0,
                                   RSPAM_VAL_DC, 1.0, VI_TRUE);

  /*
```

```
  Configure channel CHA1 for 1 MOhm impedance, no lowpass filter
*/
status = rspam_ConfigureChanCharacteristics (vi, "CHA1", 1.0e6, 20.0e6);


/*
  Configure the trigger:
  - Edge trigger
  - Trigger level 2.5 V, positive slope
*/
status = rspam_ConfigureTriggerPath (vi ,RSPAM_VAL_PATH_A,
                                     RSPAM_VAL_EDGE_TRIGGER );

status = rspam_ConfigureTriggerSourcePath (vi, RSPAM_VAL_PATH_A,
                                           "CHA1", 2.5,
                                           RSPAM_VAL_POSITIVE);


/*
  Configure the path for floating acquisition
*/
status = rspam_ConfigureGroundPath (vi, RSPAM_VAL_PATH_A, VI_FALSE);


/*
  Connect the instrument to the front connector
  and wait until all relays have been closed
*/
status = rspam_Connect (vi, "CHA1_HI", "CHA1_HI1");
status = rspam_Connect (vi, "CHA_LO",  "CHA_LO1");
status = rspam_WaitForDebounce ( vi, 1000 );


/*
  Get the actual number of points for the acquisition and allocate
  memory for it. Note that this value may be greater than the minimum
  number of samples requested above.
*/
status = rspam_ActualRecordLengthPath (vi, RSPAM_VAL_PATH_A,
                                       &actualPoints);
pWaveform = calloc (actualPoints, sizeof(ViReal64));


/*
  Start the acquisition
  - Timeout is 1000 ms
*/
status = rspam_ReadWaveform (vi, "CHA1", actualPoints, 1000,
                             pWaveform, &actualPoints, &initialX,
                             &xIncrement);


/*
  Display the wave form
*/
status = WaveformGraphPopup ("Waveform", pWaveform, actualPoints,
                             VAL_DOUBLE, 1.0, 0.0, initialX,
                             xIncrement);


/*
  Close the driver session
*/
status = rspam_close ( vi );


/*
```

```
    free memory
  */
  free ( pWaveform );

  return 0;
}
```

8 Self-test

The Analyzer Module TS-PAM has integrated self-test capability. The following tests are possible:

- LED Test
- Power-on test
- Self-test by the driver

8.1 LED Test

When the device is switched on, all three LEDs are lit for about one second. This indicates that the 5 V supply voltage is present and all LEDs are working, also that the power-on test was successful. The following statements can be made about the different LED statuses in this power-on phase:

LED	Description
One LED does not light up	Hardware problem on the module LED faulty
No LED's light up	No +5V supply

Table 8-1 Statements about the LED Test

NOTE:

If diagnostics suggest a problem with the supply voltage, the LEDs for the associated rear I/O module, TS-PDC, must be inspected visually. If a supply voltage failure is confirmed, the TS-PDC module must be replaced.

8.2 Power-on test

The power-on test runs at the same time as the LED test. In this test, the result of the FPGA loading process is calculated. The following statements can be made about the different statuses of the red and green LEDs:

LED	Description
Green LED on	all supply voltages present
green LED off	at least one supply voltage from TS-PAM module or the TS-PDC module is not present
red LED off	no errors were detected
red LED on	The FPGA/µP was not successfully loaded

Table 8-2 Statements about the power-on test

NOTE:

If diagnostics suggest a problem with the supply voltage, the LEDs for the associated rear I/O module, TS-PDC, must be inspected visually. If a supply voltage failure is confirmed, the TS-PDC module must be replaced.

8.3 Self-test by the driver

The driver which is supplied has a more extensive self-test. It is started through the standard self-test function and delivers a “PASS” or “FAIL” result.

In the TSVP self-test, a test report is generated.

NOTE:

Information on starting the self-test and on the sequence of the necessary steps can be found in the GTSL software description or the GTSL online help.

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9 Interface Description

9.1 Interface Description TS-PAM

9.1.1 Connector X1

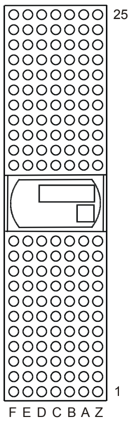

Figure 9-1 Connector X1 (view: plug side)

Pin	F	E	D	C	B	A	Z	
25	GND	5V	3.3V	ENUM#	REQ64#	5V	GND	
24	GND	ACK64#	AD[0]	V(I/O)	5V	AD[1]	GND	
23	GND	AD[2]	5V	AD[3]	AD[4]	3.3V	GND	
22	GND	AD[5]	AD[6]	3.3V	GND	AD[7]	GND	
21	GND	C/BE[0]#	M66EN	AD[8]	AD[9]	3.3V	GND	
20	GND	AD[10]	AD[11]	V(I/O)	GND	AD[12]	GND	
19	GND	AD[13]	GND	AD[14]	AD[15]	3.3V	GND	X1
18	GND	C/BE[1]#	PAR	3.3V	GND	SERR#	GND	
17	GND	PERR#	GND	IPMB_SDA	IPMB_SCL	3.3V	GND	C
16	GND	LOCK#	STOP#	V(I/O)	GND	DEVSEL#	GND	O
15	GND	TRDY#	BD_SEL#	IRDY#	FRAME#	3.3V	GND	N
12..14	Key Area							N
11	GND	C/BE[2]#	GND	AD[16]	AD[17]	AD[18]	GND	E
10	GND	AD[19]	AD[20]	3.3V	GND	AD[21]	GND	C
9	GND	AD[22]	GND	AD[23]	IDSEL	C/BE[3]#	GND	T
8	GND	AD[24]	AD[25]	V(I/O)	GND	AD[26]	GND	O
7	GND	AD[27]	GND	AD[28]	AD[29]	AD[30]	GND	R
6	GND	AD[31]	CLK	3.3V	GND	REQ#	GND	
5	GND	GNT#	GND	RST#	BSRSV	BSRSV	GND	
4	GND	INTS	INTP	V(I/O)	HEALTHY#	IPMB_PWR	GND	
3	GND	INTD#	5V	INTC#	INTB#	INTA#	GND	
2	GND	TDI	TDO	TMS	5V	TCK	GND	
1	GND	5V	+12V	TRST#	-12V	5V	GND	

Table 9-1 Pin assignment for connector X1

9.1.2 Connector X20

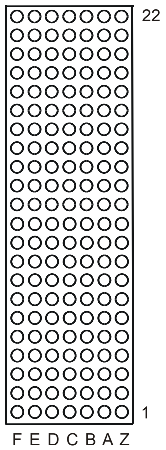

Figure 9-2 Connector X20 (view: plug side)

NC = not connected, NP = not populated

Pin	F	E	D	C	B	A	Z	
22	GND	GA0	GA1	GA2	GA3	GA4	GND	
21	GND				GND		GND	
20	GND		GND				GND	
19	GND				GND		GND	
18	GND	PXI_TRIG6	GND (CAN-En)	PXI_TRIG5	PXI_TRIG4	PXI_TRIG3	GND	X20
17	GND	PXI_CLK10			GND	PXI_TRIG2	GND	
16	GND	PXI_TRIG7	GND		PXI_TRIG0	PXI_TRIG1	GND	
15	GND				GND		GND	
14	NC						NC	C
13	NC						NC	O
12	NP	COM_1	+3.3V_1	+5V_1	-15V_1	+15V_1	NP	N
11	NP						NP	N
10	NC	COM_2	+3.3V_2	+5V_2	-15V_2	+15V_2	NC	E
9	NC						NC	C
8	NC						NC	T
7	NC						NC	O
6	NC						NC	R
5	NC						NC	
4	GND						GND	
3	GND	RSA0	RRST#		GND	RSDO	GND	
2	GND		RSDI	RSA1		RSCLK	GND	
1	GND				GND	RCS#	GND	

Table 9-2 Pin assignment for connector X20

9.1.3 Connector X10

Plug type DIN 41612, 96 pin, female

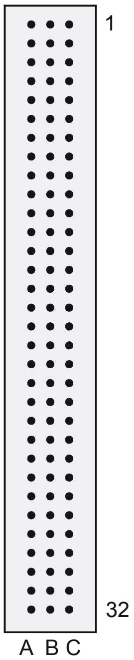

Figure 9-3 Connector X10 (view: front panel)

	A	B	C
1	LABA1	GND	LABA2
2	LABB1	GND	LABB2
3	LABC1	GND	LABC2
4	LABD1	GND	LABD2
5			
6	CHA1_HI1	CHA1_HI2	CHA1_HI3
7	CHA_LO1	CHA_LO1	CHA_LO1
8	CHA2_HI1	CHA2_HI2	CHA2_HI3
9	CHA_LO1	CHA_LO1	CHA_LO1
10			
11	CHA3_HI1	CHA3_HI2	CHA3_HI3
12	CHA_LO1	CHA_LO1	CHA_LO1
13	CHA4_HI1	CHA4_HI2	CHA4_HI3

Table 9-3 Pin assignment for connector X10 (view front panel)

	A	B	C
14	CHA_LO1	CHA_LO1	CHA_LO1
15			
16	CHB1_HI1	CHB1_HI2	CHB1_HI3
17	CHB_LO1	CHB_LO1	CHB_LO1
18	CHB2_HI1	CHB2_HI2	CHB2_HI3
19	CHB_LO1	CHB_LO1	CHB_LO1
20			
21	CHB3_HI1	CHB3_HI2	CHB3_HI3
22	CHB_LO1	CHB_LO1	CHB_LO1
23	CHB4_HI1	CHB4_HI2	CHB4_HI3
24	CHB_LO1	CHB_LO1	CHB_LO1
25			
26			
27			
28	GND	GND	GND
29	XTO1	GND	XTO2
30	XTI1	GND	XTI2
31	GND	GND	GND
32	GND	GND	CHA_GND

Table 9-3 Pin assignment for connector X10 (view front panel)

Comment:

The signal CHA_GND is connected with the front panel of the component and through two 10 nF condensers with GND. The front panel itself has no direct connection to GND. During the connection of a unit under test, the unit under test's GND should be connected to GND. Do not connect GND and CHA_GND to prevent hum loops.

9.1.4 Connector X30

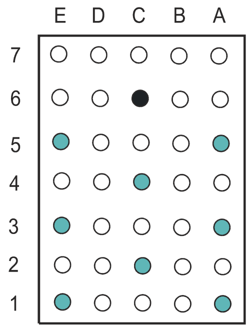

Figure 9-4 Connector X30 (view: plug side)

Pin	E	D	C	B	A
7					
6			GND		
5	ABC1				ABA1
4			ABB1		
3	ABC2				ABB2
2			ABA2		
1	ABD2				ABD1

Table 9-4 Pin assignment for connector X30

9.2 Interface Description TS-PDC

9.2.1 Connector X20 (Extension Connector)

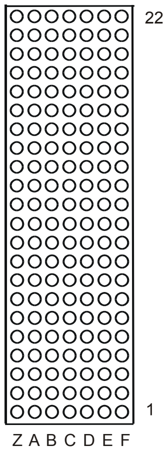

Figure 9-5 Connector X20 (view: plug side TS-PDC)

Pin	Z	A	B	C	D	E	F	
22	GND						GND	
21	GND		GND or NC *3)				GND	
20	GND			+5V *1)	GND	+5V *1)	GND	
19	GND		GND	+5V *1)			GND	
18	GND				GND		GND	J20
17	GND		GND	+5V *2)	+5V *2)		GND	
16	GND			+5V *2)	GND		GND	
15	GND		GND	+5V *2)	+5V *1)		GND	
14	NC						NC	C
13	NC						NC	O
12	NP	+15V_1	-15V_1	+5V_1	+3.3V_1	COM_1	NP	N
11	NP						NP	N
10	NC	+15V_2	-15V_2	+5V_2	+3.3V_2	COM_2	NC	E
9	NC						NC	C
8	NC	COM_1	COM_1	COM_1	COM_1	COM_1	NC	T
7	NC						NC	O
6	NC	COM_2	COM_2	COM_2	COM_2	COM_2	NC	R
5	NC						NC	
4	NC						NC	
3	GND		GND		RRST#		GND	
2	GND	RSCLK			RSDI		GND	
1	GND	RCS#	GND			+5V *1)	GND	
Pin	Z	A	B	C	D	E	F	

*1) TS-PDC V1.0 is supplied via these pins from +5V, for backplanes up to V3.x
*2) TS-PDC V1.1 is supplied via these pins or pins from *1) , for backplanes V1.x to V4.x
*3) TS-PDC V1.1 and V1.2: GND, for version V1.3: NC (Not Connected)

Table 9-5 Pin assignment for connector X20 (TS-PDC)

10 Technical Data

NOTE:

The technical data of the Analyzer Modules TS-PAM and the Rear I/O Module TS-PDC are shown in the corresponding data sheets.

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